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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/808,627	03/24/2004	Nui Chong	M-15338 US	6086

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EXAMINER	
PATEL, DHARTI HARIDAS	

ART UNIT	PAPER NUMBER
2836	

DATE MAILED: 10/11/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/808,627	CHONG ET AL.	
	Examiner	Art Unit	
	Dharti H. Patel	2836	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *13 July 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-22* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-22* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *24 March 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

1. Claims 1-4, 8-12, 14, 16-20, and 22 are rejected under 35 U.S.C. 102(e) as being anticipated by Mergens et al., Patent No. 6,768,616.

With respect to claim 1, Mergens teaches a circuit [Fig. 20] comprising a diode string [Fig. 20, 2008] coupled to a supply voltage line [Fig. 20, 2004]; a transistor [Fig. 20, 312] coupled to the diode string [Fig. 20, 2008] and to a reference voltage line [Fig. 20, 112; Transistor 312 is coupled to a reference voltage line 112 via resistor 341], wherein the diode string and the transistor are implemented in a cascode configuration and provide electrostatic discharge protection [Col. 13, lines 59-60, Col. 14, lines 1-3]; and wherein the diode string comprises a first diode [Fig. 20; the first diode connected to the supply voltage line in a diode string 2008] coupled between the supply voltage line [Fig. 20, 2004] and the transistor [Fig. 20, 312] and disposed such that the first diode is forward biased from the supply voltage line to the transistor, wherein the first

diode is adapted to provide electrostatic discharge protection having a first polarity; and a second diode [Fig. 20, a first diode connected to the power supply 2004, in a diode string 2010] coupled to the supply voltage line [Fig. 20, 2004] and the transistor and parallel to the first diode, wherein the second diode is adapted to provide electrostatic discharge protection having a second polarity.

With respect to claim 2, Mergens teaches that the diode string [Fig. 20, 2009] further comprises a third diode [Fig. 20; The diode connected to the transistor in a diode string 2008] arranged in series with the first diode with a cathode of the first diode coupled to an anode of the third diode, and wherein the second diode is further in parallel with the transistor as disclosed in Fig. 20.

With respect to claim 3, Mergens teaches that the second diode has at least a first terminal coupled to a drain terminal of the transistor [Fig. 20, 312].

With respect to claim 4, Mergens teaches that the transistor [Fig. 20, 312] and the diode string [Fig. 20, 2008] have different diffusion regions.

With respect to claim 8, Mergens teaches that the circuit is adapted to operate in a mixed voltage environment [Fig. 20].

With respect to claim 9, Mergens teaches that one or more diodes [Fig. 20, 2008] within the diode string may be implemented as bipolar transistors.

With respect to claim 10, Mergens teaches a programmable logic device [Fig. 20] comprising at least a first diode [Fig. 20; the first diode connected to the supply voltage line in a diode string 2008] coupled between a supply voltage line [Fig. 20, 2004] and a reference voltage line [Fig. 20, 112] and having an anode

coupled to the supply voltage line, wherein the at least first diode is adapted to protect from electrostatic discharge of a first polarity; at least a second diode [Fig. 20, a first diode connected to the power supply 2004, in a diode string 2010] coupled between the supply voltage line [Fig. 20, 2004] and the reference voltage line [Fig. 20, 112] and in parallel with the at least first diode, wherein the at least second diode is adapted to protect from electrostatic discharge of a second polarity; and a transistor [Fig. 20, 312] coupled between the at least first diode and the reference voltage line.

With respect to claim 11, Mergens teaches that the transistor [Fig. 20, 312] and the at least first diode are implemented in a cascode configuration and adapted to operate in a mixed voltage environment.

With respect to claim 12, Mergens teaches that the transistor [Fig. 20, 312] and the at least first diode have different diffusion regions.

With respect to claim 14, Mergens teaches that the at least second diode has a first terminal coupled to a drain terminal of the transistor as disclosed in Fig. 20.

With respect to claim 16, Mergens teaches that the at least first diode and/or the at least second diode comprise a bipolar transistor [Fig. 20; the diodes can be implemented as bipolar transistors].

With respect to claim 17, Mergens teaches a method of providing electrostatic discharge protection [Fig. 20], the method comprising providing at least a first diode [Fig. 20; the first diode connected to the supply voltage line in a

diode string 2008] having an anode coupled to a supply voltage rail [Fig. 20, 2004] to protect from electrostatic discharge of a first polarity; providing a transistor [Fig. 20, 312] coupled between the at least first diode and a reference voltage rail [Fig. 20, ground]; and providing at least a second diode [Fig. 20, a first diode connected to the power supply 2004, in a diode string 2010] coupled to the supply voltage rail and to the transistor to protect from electrostatic discharge of a second polarity, wherein the at least first diode and the transistor are implemented in a cascode configuration.

With respect to claim 18, Mergens teaches that the at least first diode and the transistor [Fig. 20, 312] are implemented having different diffusions.

With respect to claim 19, Mergens further comprises operating the at least first diode, the at least second diode, and the transistor as a clamp circuit as disclosed in Fig. 20.

With respect to claim 20, Mergens further comprises operating the at least first diode, the at least second diode, and the transistor as a driver to transfer data via a pad as disclosed in Fig. 20.

With respect to claim 22, Mergens teaches that at least first diode and/or the at least second diode comprise a bipolar transistor [Fig. 20; The diodes can be implemented as bipolar transistors].

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 5-7, 13, 15, and 21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Mergens et al., Patent No. 6,768,616, in view of applicant's acknowledged prior art.

Mergens teaches an ESD protection circuit, but does not disclose that the ESD circuit further comprises a resistor coupled between a gate terminal of the transistor and the reference voltage line.

With respect to claim 5, the acknowledged prior art [Fig. 1a] teaches an ESD protection circuit, which comprises a resistor [Fig. 1a, 106] coupled between a gate terminal of the transistor [Fig. 1a, 104] and the reference voltage line [Fig. 1a, Ground], wherein the circuit provides electrostatic discharge protection for a power rail of an integrated circuit incorporating the circuit.

Both teachings are analogous electrostatic discharge protection circuits. It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of the acknowledged prior art, which teaches a resistor coupled between the transistor and ground, with the ESD circuit of Mergens, for the benefit of draining the ESD current to ground via resistor.

With respect to claim 6, the acknowledged prior art further comprises a pull-up circuit [Fig. 1b, 108] coupled between the supply voltage line [Fig. 1b, VCC] and the diode string [Fig. 1b 110, 112; the transistors can be implemented

as a diode string], wherein the pull-up circuit [Fig. 1b, 108] and the diode string are coupled to an input pad [Fig. 1b, PAD] and/or an output pad, the transistor is adapted to receive a control signal [Fig. 1b, VCTRL] at its gate terminal [Fig. 1b; gate terminal of transistor 112], and the circuit provides electrostatic discharge protection for an interface of an integrated circuit incorporating the circuit.

With respect to claim 7, the acknowledged prior art teaches that the circuit is adapted to operate as a driver [Specifications, page 2, lines 20-21].

With respect to claim 13, the acknowledged prior art teaches that the circuit further comprises a resistor [Fig. 1a, 106] coupled between a gate terminal of the transistor [Fig. 1a, 104] and the reference voltage line [Fig. 1a, ground]. The resistor, the at least first diode, the at least second diode, the transistor provide electrostatic discharge protection for a power rail of the circuit.

With respect to claim 15, the acknowledged prior art further comprises a pull-up circuit [Fig. 1b, 108] coupled between the supply voltage line [Fig. 1b, VCC] and at least first diode [Fig. 1b 110; transistor can be implemented as a diode], wherein the pull-up circuit [Fig. 1b, 108] and the at least first diode are coupled to a pad [Fig. 1b, PAD], the transistor is adapted to receive a control signal [Fig. 1b, VCTRL] at its gate terminal [Fig. 1b; gate terminal of transistor 112], and the at least first diode, the at least second diode, and the transistor provide electrostatic discharge protection for the circuit.

With respect to claim 21, the acknowledged prior art [Fig. 1b] further comprises providing a pull-up circuit [Fig. 1b, 108] between the supply voltage rail [Fig. 1b, VCC] and the at least first diode [Fig. 1b, 110].

Response to Arguments

3. Applicant's arguments with respect to claims 1-22 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

4. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dharti H. Patel whose telephone number is 571-272-8659. The examiner can normally be reached on 8:30am - 5pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Brian Sircus can be reached on 571-272-2800, Ext. 36. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service

Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

DHP
09/28/2006

Stephen W Jackson
10/2/06

STEPHEN W. JACKSON
PRIMARY EXAMINER